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【書類名】圖面

~~FIG. 1~~ FIG. I

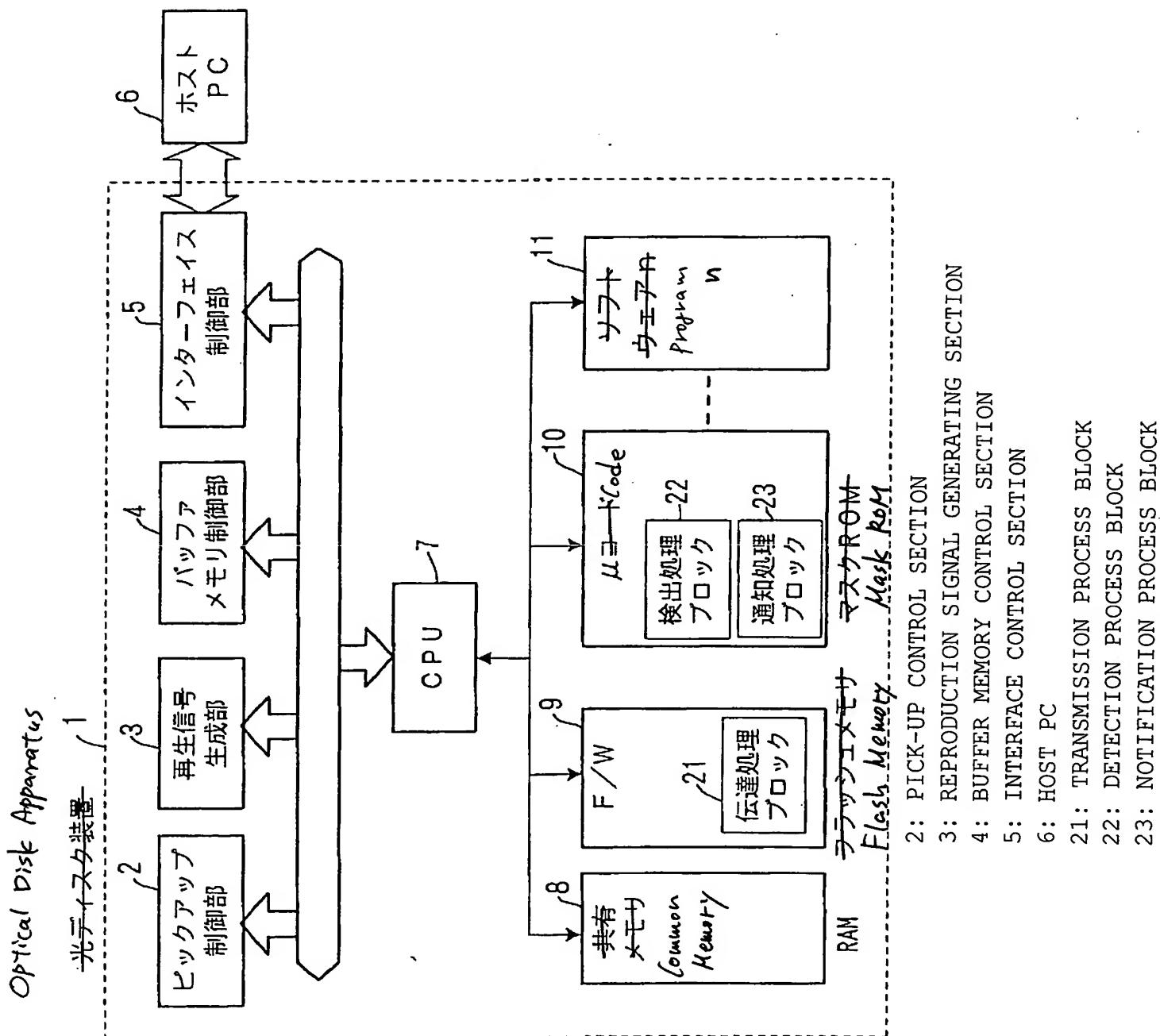
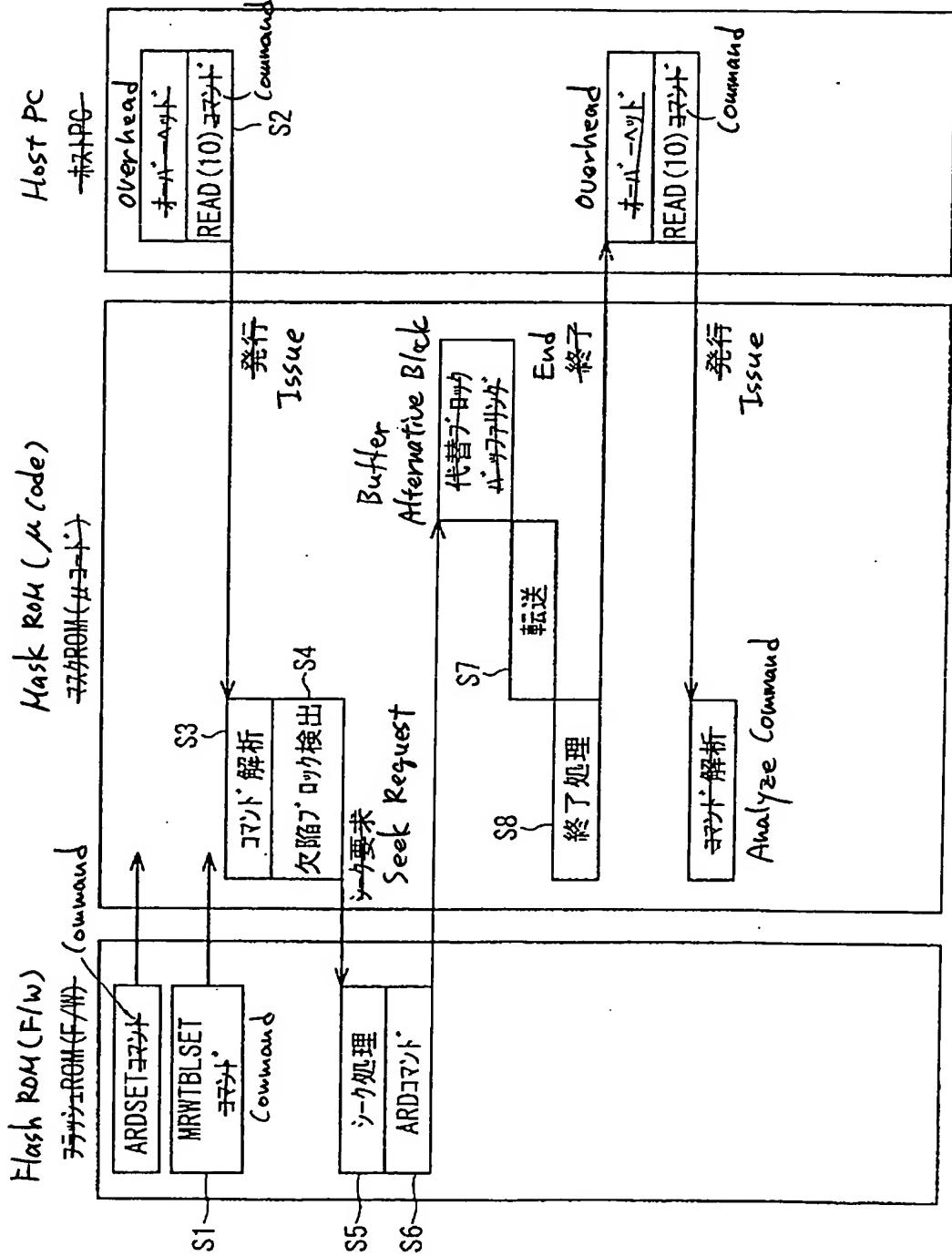
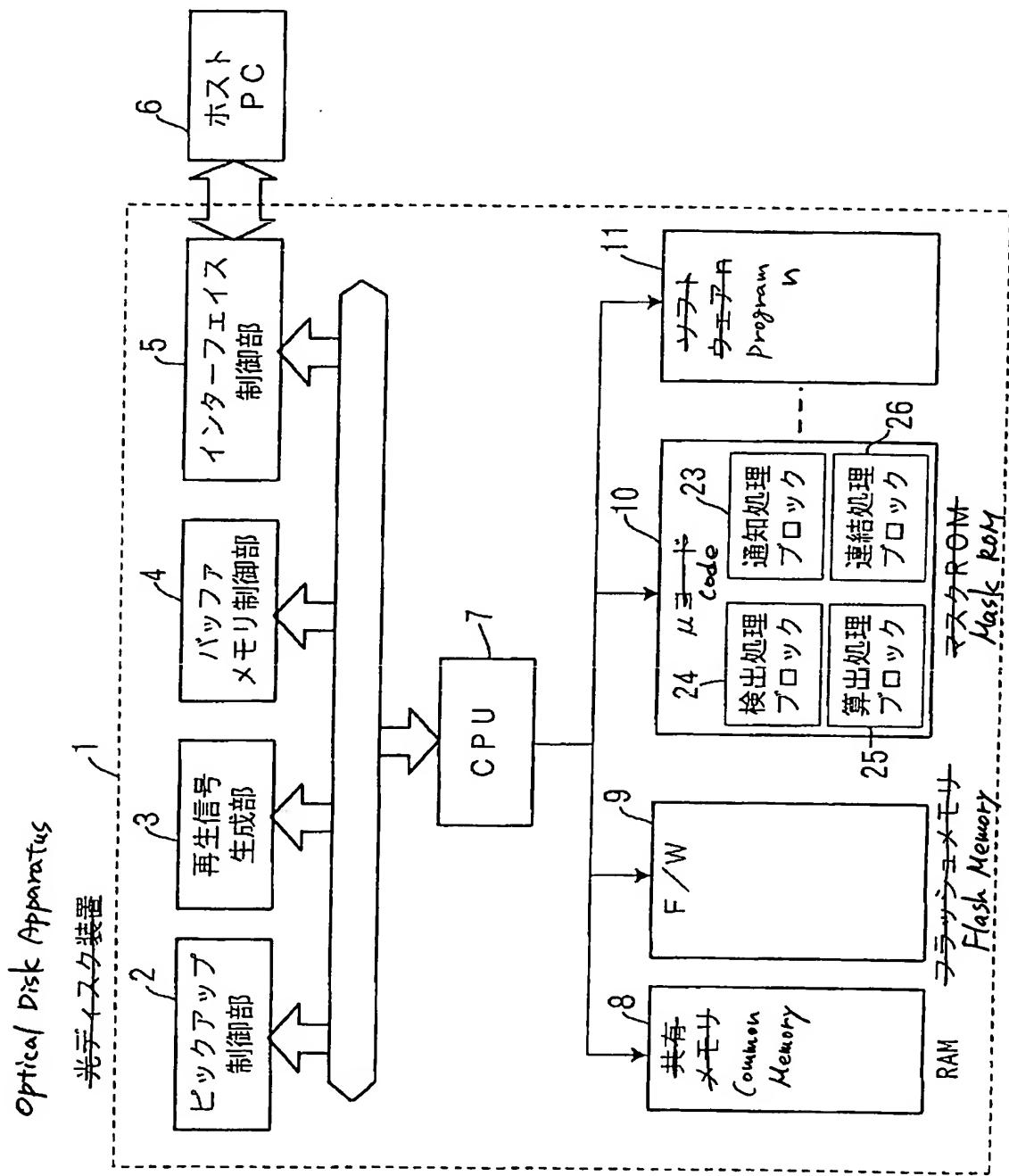


図2 FIG. 2



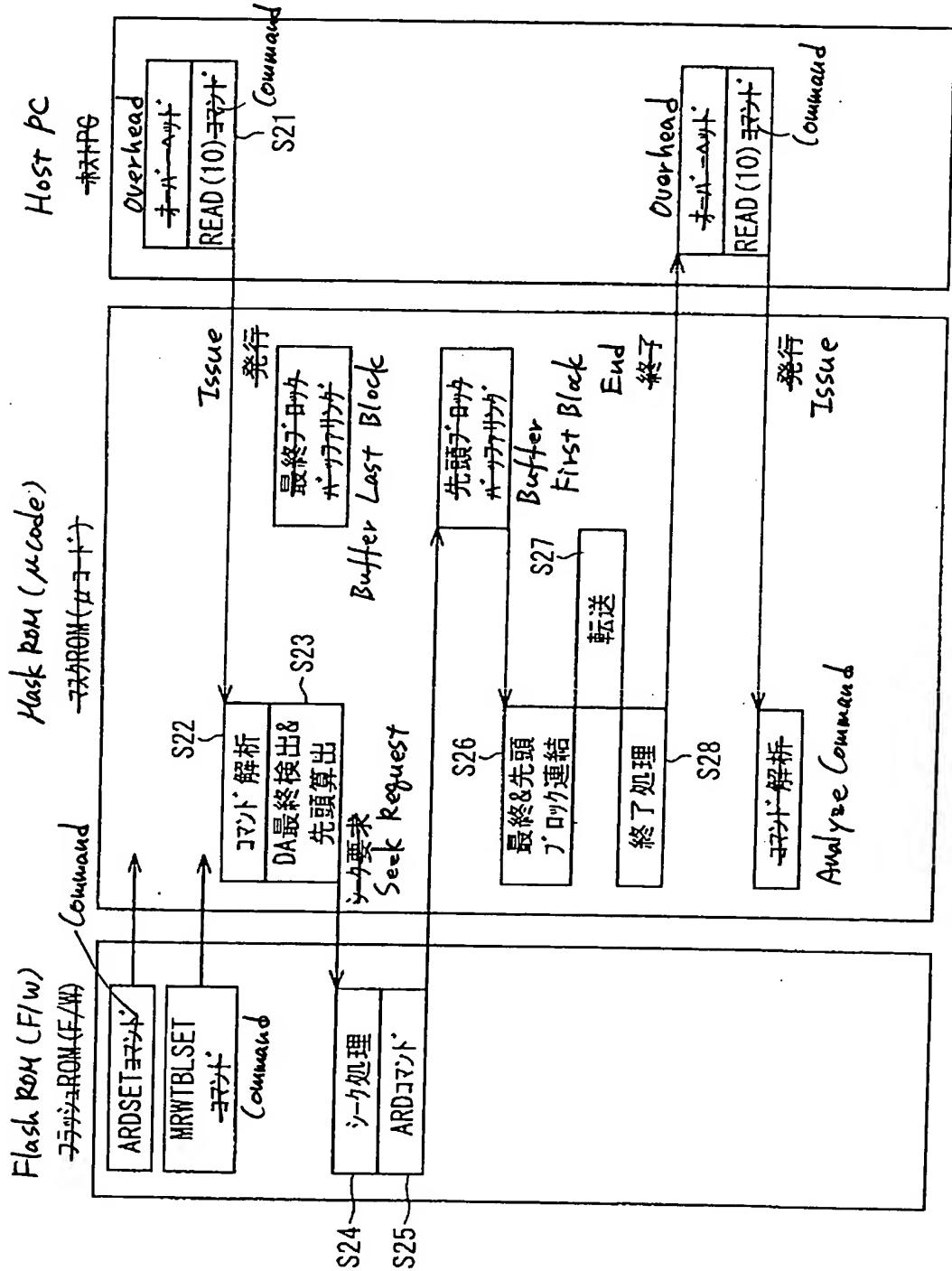
S3: ANALYZE COMMAND
 S4: DETECT DEFECTIVE BLOCK
 S5: SEEK PROCESS
 S6: ARD COMMAND
 S7: TRANSFER
 S8: TERMINATING PROCESS

十図3 FIG.3



- 2: PICK-UP CONTROL SECTION
- 3: REPRODUCTION SIGNAL GENERATING SECTION
- 4: BUFFER MEMORY CONTROL SECTION
- 5: INTERFACE CONTROL SECTION
- 6: HOST PC
- 23: NOTIFICATION PROCESS BLOCK
- 24: DETECTION PROCESS BLOCK
- 25: CALCULATION PROCESS BLOCK
- 26: CONNECTING PROCESS BLOCK

図4 FIG. 4



S22: ANALYZE COMMAND
 S23: DETECT END OF DA AND CALCULATE HEAD OF NEXT DA
 S24: SEEK PROCESS
 S25: ARD COMMAND
 S26: CONNECT END AND FIRST BLOCKS
 S27: TRANSFER
 S28: TERMINATING PROCESS

~~(图5)~~ FIG. 5

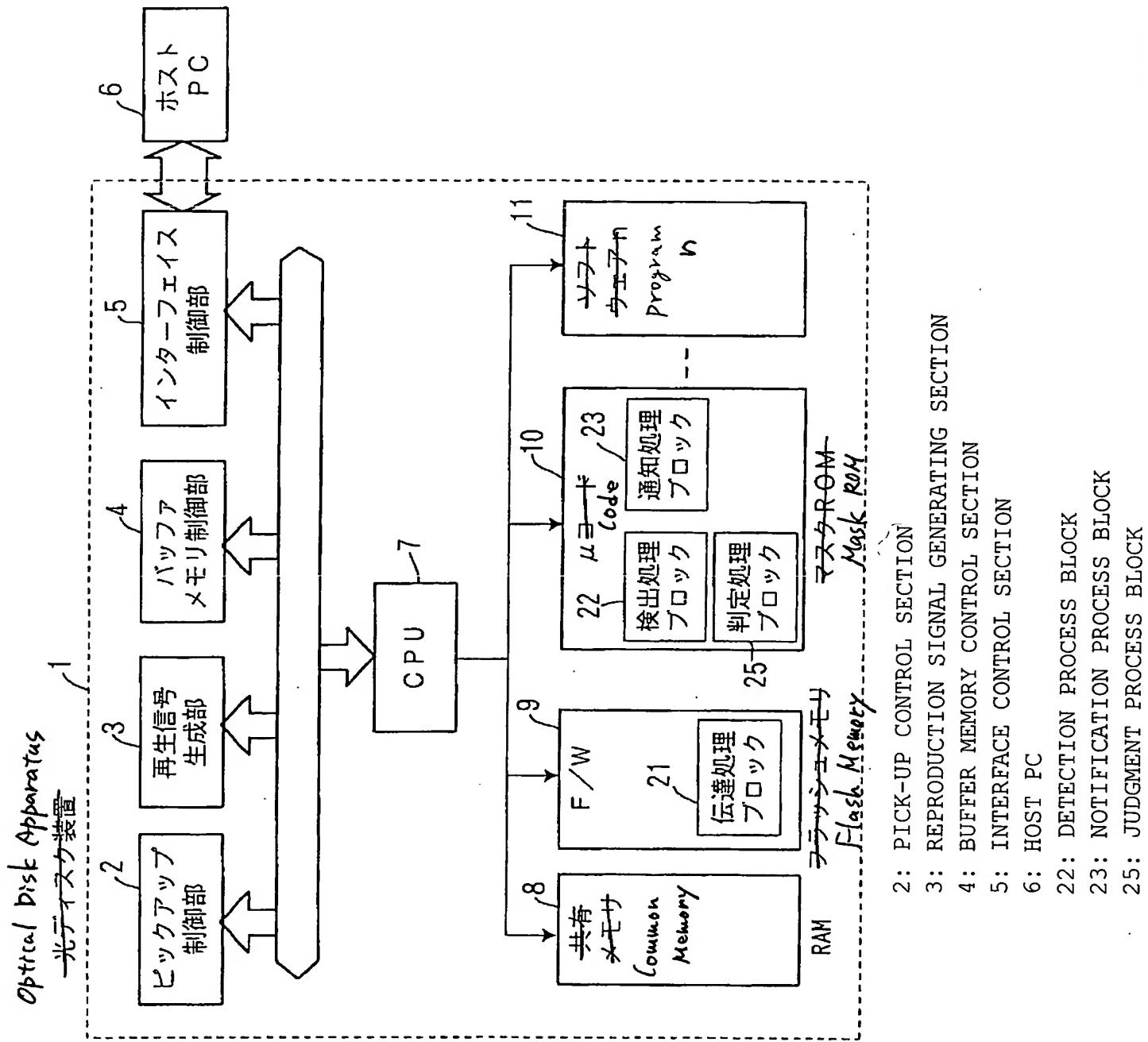
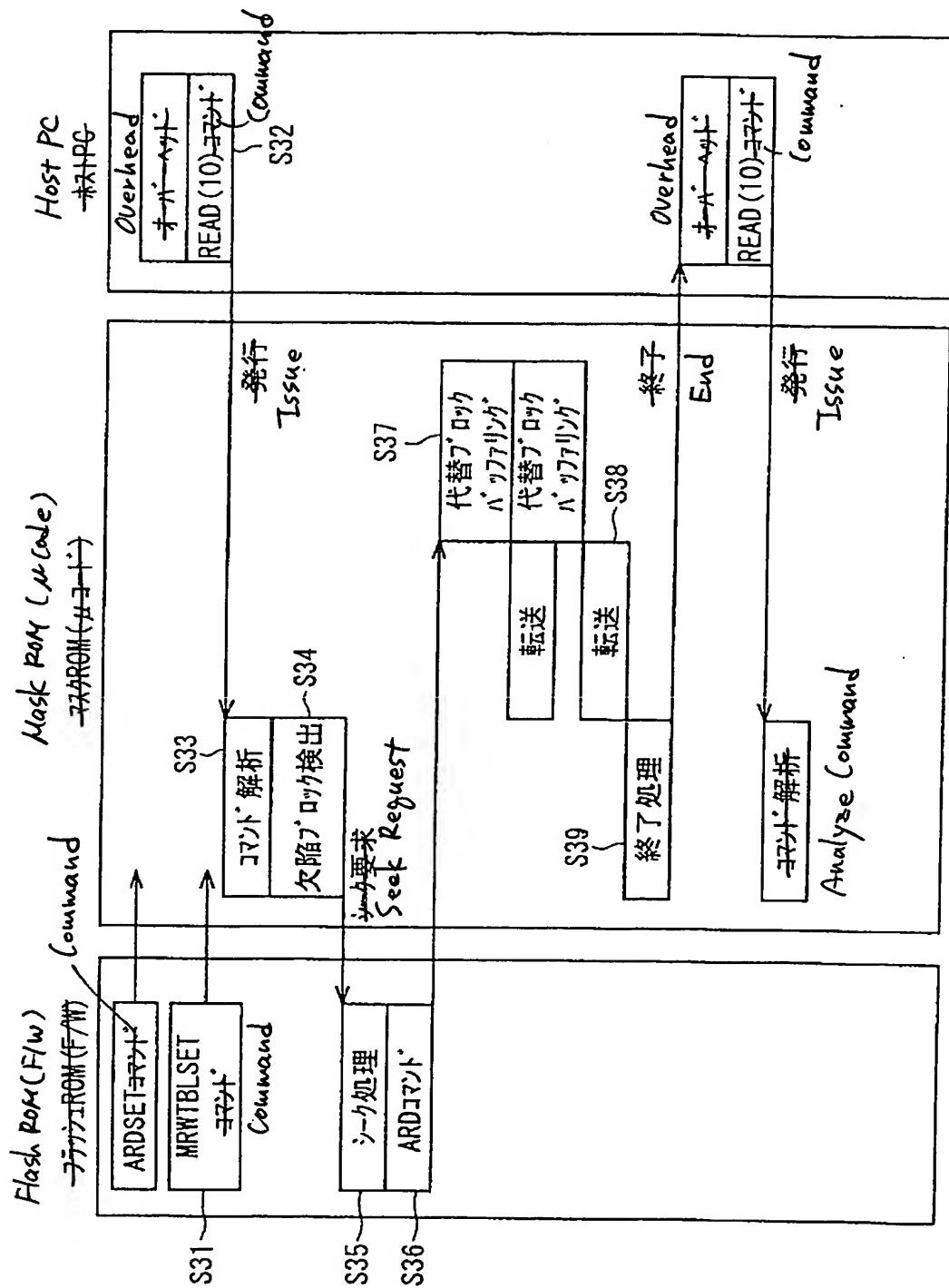
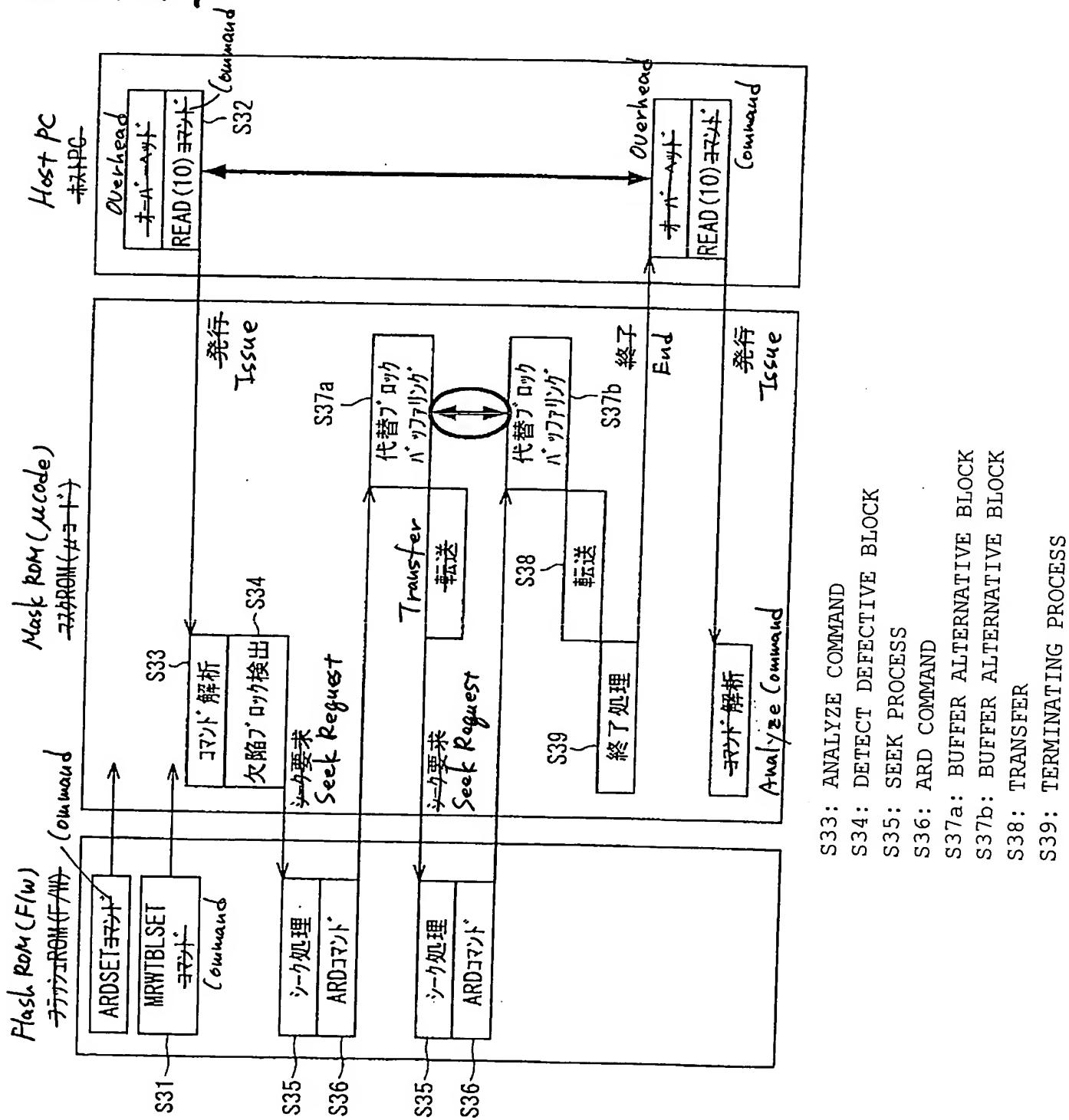


図6 FIG. 6



S33: ANALYZE COMMAND
 S34: DETECT DEFECTIVE BLOCK
 S35: SEEK PROCESS
 S36: ARD COMMAND
 S37: BUFFER ALTERNATIVE BLOCK
 S38: TRANSFER
 S39: TERMINATING PROCESS

図7 FIG. 7



S33: ANALYZE COMMAND

S34: DETECT DEFECTIVE BLOCK

S35: SEEK PROCESS

S36: ARD COMMAND

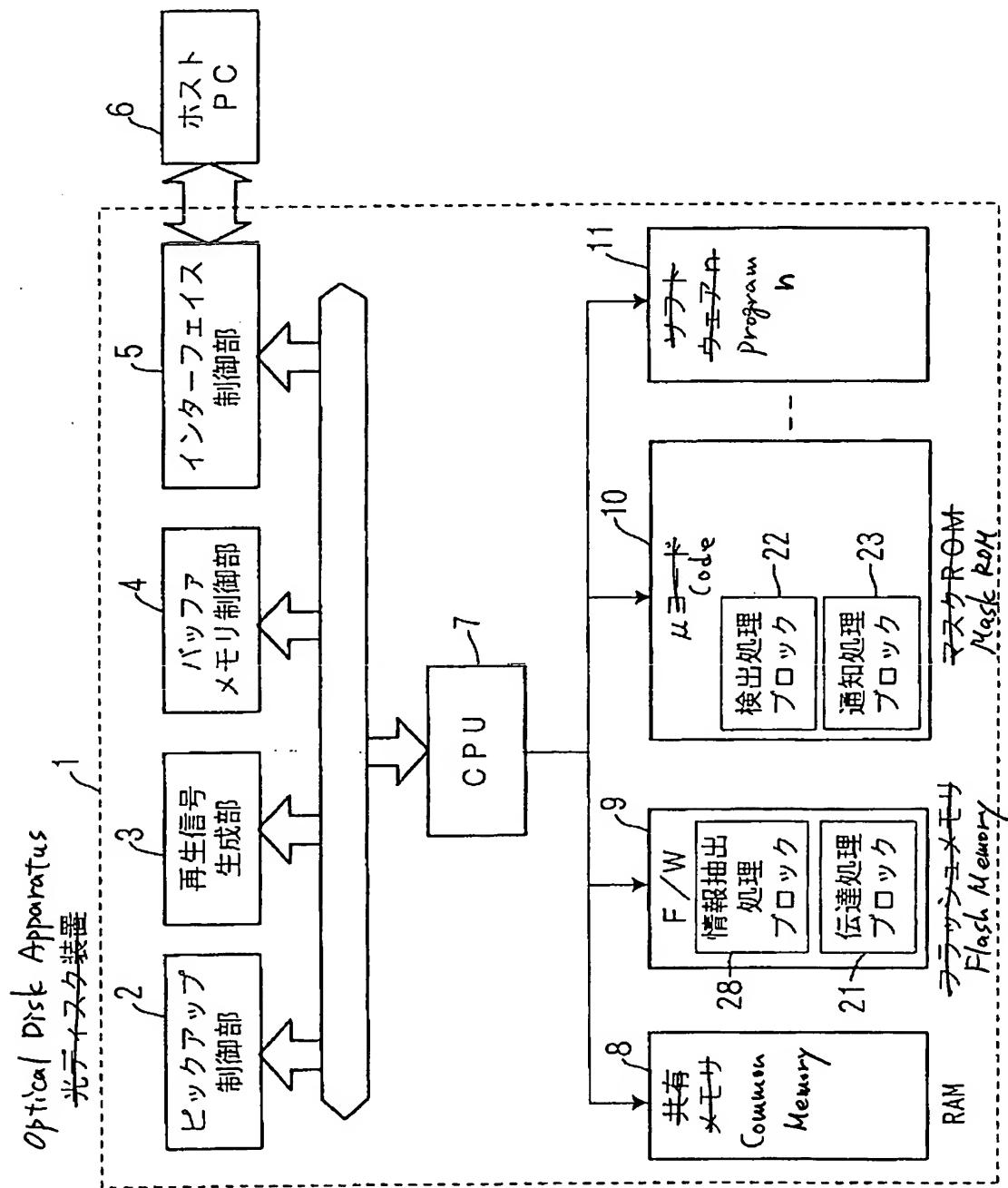
S37a: BUFFER ALTERNATIVE BLOCK

S37b: BUFFER ALTERNATIVE BLOCK

S38: TRANSFER

S39: TERMINATING PROCESS

図8 FIG.8



- 2: PICK-UP CONTROL SECTION
- 3: REPRODUCTION SIGNAL GENERATING SECTION
- 4: BUFFER MEMORY CONTROL SECTION
- 5: INTERFACE CONTROL SECTION
- 6: HOST PC
- 21: TRANSMISSION PROCESS BLOCK
- 22: DETECTION PROCESS BLOCK
- 23: NOTIFICATION PROCESS BLOCK
- 28: INFORMATION EXTRACTING PROCESS BLOCK

[図9]

FIG. 9A

Defective Block (a)

Alternative Block

MOT	DTB	Status 1 次回プロック PBN	Status 2 次回プロック PBN
0	0	0 05 A0	x xx xx
		1 06 73	x xx xx
		0/1 昇順位 1	x xx xx
		0 0F 73	x xx xx
		-2 0 00 00	x 0 04 00
		2 0 00 00	x 0 04 01
		2 0 00 00	x 0 04 02
		2 0 00 00	x 昇順位 1
		2 0 00 00	x 0 04 ff
		3 x xx xx	x 0 00 23
		3 x xx xx	x 任意の順位 1
		3 x xx xx	x 0 02 05
1	1	0 1F 73	x xx xx
	0/1 昇順位 1	x xx xx	
	:	:	:
	2	0 00 00	x > 0 04 FF
	2	0 00 00	x 昇順位 1
	:	:	:
	3	x xx xx	x xx xx
	:	:	:
2	0/1	etc	
	:	:	:
	2	0 00 00	x etc
	:	:	:
	3	x xx xx	x xx xx
	:	:	:

FIG. 9B

(b)

00 00 05 A0	xx xx xx xx
00 10 06 75	xx xx xx xx
昇順位 1	xx xx xx xx
00 00 0F 75	xx xx xx xx
01 10 1F 75	xx xx xx xx
昇順位 1	xx xx xx xx
:	:
:	:
:	:

Value in
Ascending OrderValue in
Ascending OrderValue in
Ascending Order

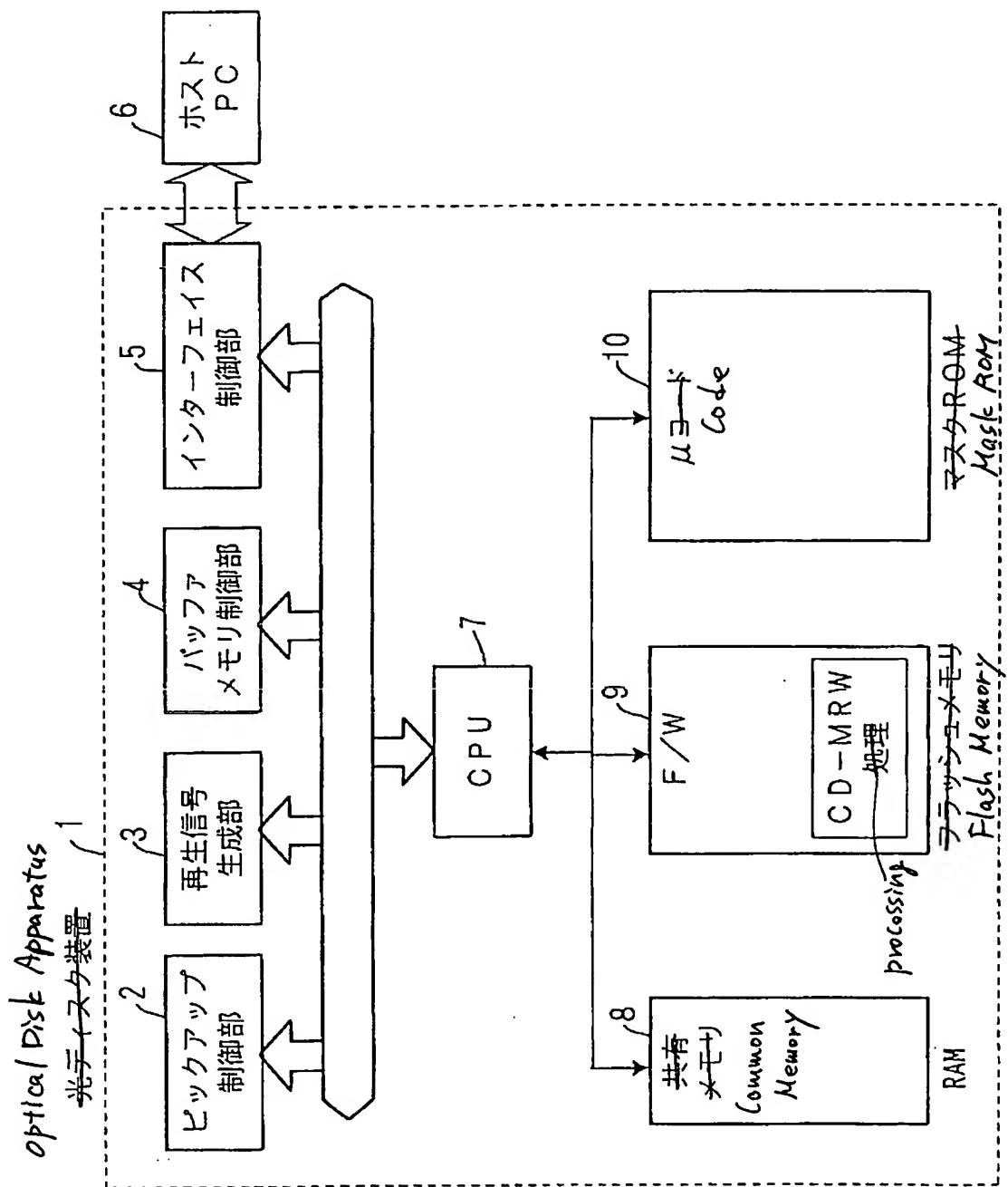
Value in Ascending Order

Arbitrary Order

Value in Ascending Order

Value in Ascending Order

十図10 FIG. 10



- 2: PICK-UP CONTROL SECTION
- 3: REPRODUCTION SIGNAL GENERATING SECTION
- 4: BUFFER MEMORY CONTROL SECTION
- 5: INTERFACE CONTROL SECTION
- 6: HOST PC